19-0524; Rev 1; 8/06

Multiple-Output Clock Generators with Dual PLLs and OTP

General Description

The MAX9471/MAX9472 multipurpose clock generators are ideal for consumer and communication applications. The MAX9471/MAX9472 feature two buffered phase-locked loop (PLL) outputs that can be independently set from 4MHz to 200MHz. These devices also provide one (MAX9472) or two (MAX9471) buffered outputs of the reference clock.

The MAX9471 outputs a set of MPEG/AC3 audio and video frequencies most commonly used in consumer applications. The MAX9472 outputs a set of common audio frequencies. These frequencies are selected through an I²C† interface (MAX9471) or by setting the three-level FS pins. The MAX9471/MAX9472 feature a one-time-programmable (OTP) ROM, allowing one-time programming of the two PLL outputs.

The MAX9471/MAX9472 include two basic configurations. In one configuration, the OTP ROM sets PLL1 output to any frequency between 4MHz to 200MHz, and the I²C interface (MAX9471) or programmable pins set the PLL2 output frequency to a set of audio and video frequencies. In the other configuration, the OTP ROM sets both PLL1 and PLL2 frequencies to fixed values between 4MHz to 200MHz. In both cases, the reference output is available, but the OTP ROM can disable it.

The OTP ROM on the MAX9471/MAX9472 is factory set based on the customer requirements. Contact the factory for samples with preferred frequencies.

The devices operate from a 3.3V supply and are specified over the -40°C to +85°C extended temperature range. The MAX9471 is available in a 20-pin TQFN package. The MAX9472 is available in a 14-pin TSSOP package.

Applications

Digital TVs

Communication Systems

Data Networking Systems

Set-Top Boxes

Home Entertainment Centers

Multimedia PCs

†Purchase of I²C components from Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Features

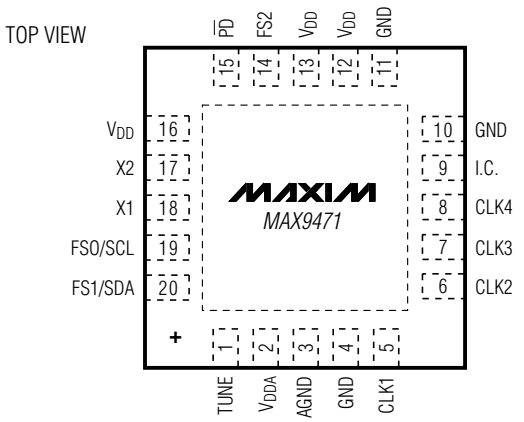
- **5MHz to 50MHz Input Clock Reference**
- **Crystal or Input-Clock-Based Reference**
- **Two Fractional-N Feedback PLLs (4MHz to 200MHz) with Buffered Outputs**
- **Two Buffered Outputs of Reference Clock**
- **OTP for Factory-Preset PLL Frequencies Available (Contact Factory)**
- **Programmable Through I²C Interface or Three-Level Logic Pins for Video or Audio Clocks**
- **Low-RMS Jitter PLL (14ps for 45MHz)**
- **Integrated VCXO with ±200ppm Tuning Range**
- **Available in 20-Pin TQFN and 14-Pin TSSOP Packages**
- **+3.3V Supply**
- **-40°C to +85°C Temperature Range**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9471ETP+**	-40°C to +85°C	20 TQFN-EP*	T2055-5
MAX9472EUD+**	-40°C to +85°C	14 TSSOP	U14-2

**EP = Exposed pad.*
***Marking is for samples only. Contact factory for ordering information.*
+Denotes lead-free package.

Pin Configurations



TQFN (5mm x 5mm)

Pin Configurations continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Multiple-Output Clock Generators with Dual PLLs and OTP

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +4.0V
V_{DDA} to AGND .....-0.3V to +4.0V
AGND to GND .....-0.3V to +0.3V
All Other Pins to GND .....-0.3V to V_{DD} + 0.3V
Short-Circuit Duration
(all LVCMOS outputs).....Continuous
ESD Protection (Human Body Model).....±2kV

Continuous Power Dissipation (T_A = +70°C)
20-Pin TQFN (derate 21.3mW/°C above +70°C) 2758mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 796.8mW
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{DDA} = +3.0V to +3.6V and T_A = -40°C to +85°C. Typical values at V_{DD} = V_{DDA} = 3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVCMOS INPUTS ($\overline{PD}$, X1 as a reference INPUT CLK)						
Input High Level	V_{IH1}		2.0		V_{DD}	V
Input Low Level	V_{IL1}		0		0.8	V
Input Current High Level	I_{IH1}	V_{IN} = V_{DD}			20	µA
Input Current Low Level	I_{IL1}	V_{IN} = 0	-20			µA
THREE-LEVEL INPUTS (FS0, FS1, FS2, as FS2 = open)						
Input High Level	V_{IH2}		2.5			V
Input Low Level	V_{IL2}				0.8	V
Input Open Level	V_{IO2}		1.27		2.10	V
Input Current	I_{IL2}, I_{IH2}	V_{IL2} = 0 or V_{IH2} = V_{DD}	-10		+10	µA
SERIAL INTERFACE (SCL, SDA) (Note 2) (MAX9471)						
Input High Level	V_{IH}		0.7 x V_{DD}			V
Input Low Level	V_{IL}				0.3 x V_{DD}	V
Input-Leakage Current	I_{IH}, I_{IL}		-1		+1	µA
Low-Level Output	V_{OL}	I_{SINK} = 4mA			0.4	V
Input Capacitance	C_I	(Note 3)		8.4		pF
CLOCK OUTPUTS (CLK_)						
Output High Level	V_{OH}	I_{OH} = -4mA	V_{DD} - 0.6			V
Output Low Level	V_{OL}	I_{OL} = 4mA			0.4	V
POWER SUPPLIES						
Digital Power-Supply Voltage	V_{DD}		3.0		3.6	V
Analog Power-Supply Voltage	V_{DDA}		3.0		3.6	V
Total Current for Digital and Analog Supplies	I_{DC}	CLK1 at 125MHz and CLK2 at 74.1758MHz; all outputs not loaded		12		mA
Total Power-Down Current	I_{PD}	$\overline{PD}$ = low		60		µA

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{DDA} = +3.0V to +3.6V, T_A = -40°C to +25°C. Typical values are at V_{DD} = V_{DDA} = 3.3V, T_A = +25°C with f_{XTL} = 27MHz, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT CLOCKS (CLK1, CLK2)						
Minimum Frequency Range	f_{OUT}	f_{IN} = 5MHz to 50MHz	4			MHz
Maximum Frequency Range	f_{OUT}	f_{IN} = 5MHz to 50MHz, C_L < 5pF	133	200		MHz
Clock Rise Time	t_R	20% to 80% of V_{DD}, C_L = 10pF, f_{OUT} = 74.1758MHz (Figure 5)		1.4		ns
Clock Fall Time	t_F	80% to 20% of V_{DD}, C_L = 10pF, f_{OUT} = 74.1758MHz (Figure 5)		1.2		ns
Duty Cycle		f_{OUT} = 74.1758MHz, C_L = 10pF	42	50	58	%
Output Period Jitter	J_P	125MHz, C_L = 5pF, f_{IN} = 27MHz		26.3		RMSps
		74.1758MHz, C_L = 10pF, f_{IN} = 27MHz		33.6		
Soft Power-On Time	t_{FST}	SDA from low to high, f_{OUT} = 71.1758MHz, f_{IN} = 13MHz (Figure 6)		1		ms
Hard Power-On Time	t_{PO1}	(Figure 6)		15		ms
VCXO CLOCKS (CLK3, CLK4)						
Crystal Frequency	f_{XTL}			27		MHz
Crystal Accuracy				±30		ppm
Tuning Voltage Range	V_{TUNE}		0.0		3.0	V
VCXO Tuning Range		V_{TUNE} = 0 to 3V, C_1 = C_2 = 4.0pF	±150	±200		ppm
TUNE Input Impedance	Z_{TUNE}			95		kΩ
Output CLK Accuracy		V_{TUNE} = 1.5V, C_1 = C_2 = 4.0pF		±50		ppm
Output Duty Cycle		C_L = 10pF load, CLK3	40	50	60	%
Output Period Jitter		C_L = 10pF		36		RMSps
Output Rise Time	t_R	20% to 80% of V_{DD} (Figure 5), C_L = 10pF		1.4		ns
Output Fall Time	t_F	80% to 20% of V_{DD} (Figure 5), C_L = 10pF		1.4		ns

Multiple-Output Clock Generators with Dual PLLs and OTP

SERIAL-INTERFACE TIMING CHARACTERISTICS (MAX9471)

(V_{DD} = V_{DDA} = +3.3V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1, Figure 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time, Repeated START Condition	$t_{HD,STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU,STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU,STO}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$	(Note 4)	15		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of SDA and SCL, Receiving	t_R	(Notes 3, 5)	$20 + 0.1C_b$		300	ns
Fall Time of SDA and SCL, Receiving	t_F	(Notes 3, 5)	$20 + 0.1C_b$		300	ns
Fall Time of SDA, Transmitting	$t_{F,TX}$	(Notes 3, 6)	$20 + 0.1C_b$		250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Notes 3, 7)	0		50	ns
Capacitive Load for Each Bus Line	C_b	(Note 3)			400	pF

Note 1: All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: No high-output level is specified, only the output resistance to the bus. Pullup resistors on the bus provide the high-level voltage.

Note 3: Guaranteed by design.

Note 4: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.

Note 5: C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3 x V_{DD} and 0.7 x V_{DD}.

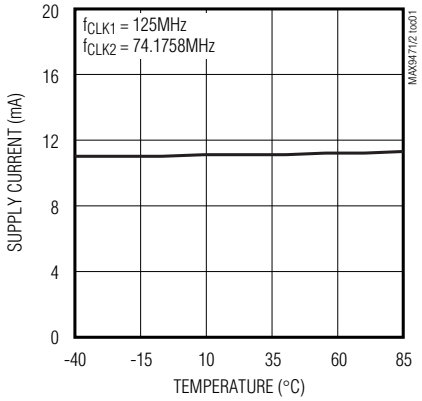
Note 6: Bus sink current is less than 6mA. C_b is the total capacitance of one bus line in pF. t_R and t_F are measured between 0.3 x V_{DD} and 0.7 x V_{DD}.

Note 7: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

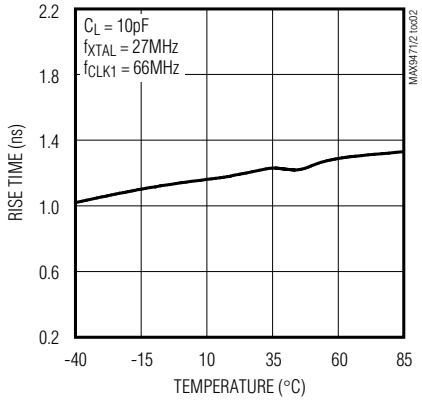
Typical Operating Characteristics

(V_{DD} = V_{DDA} = +3.3V, T_A = +25°C, f_{XTL} = 27MHz, unless otherwise noted.)

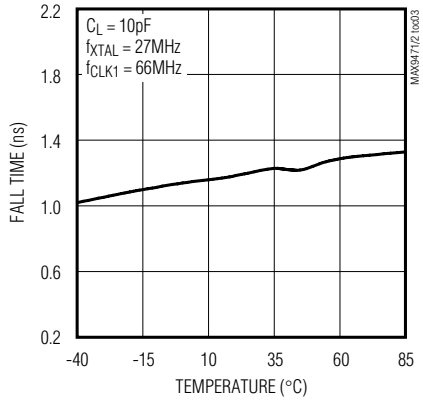
SUPPLY CURRENT vs. TEMPERATURE



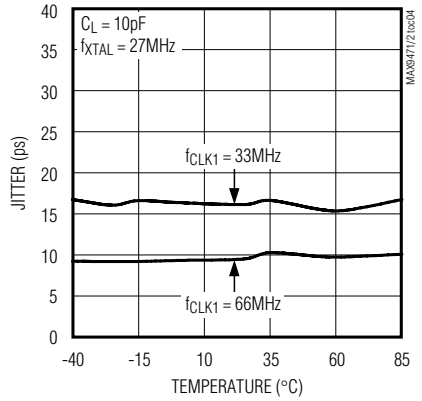
RISE TIME vs. TEMPERATURE



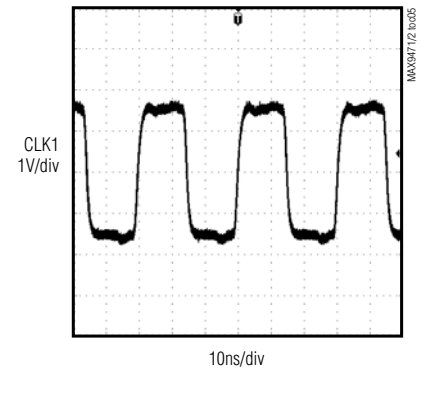
FALL TIME vs. TEMPERATURE



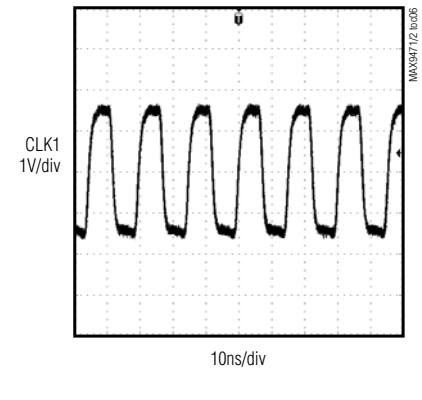
JITTER vs. TEMPERATURE



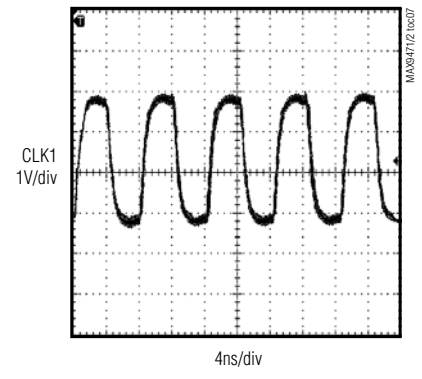
33MHz OUTPUT



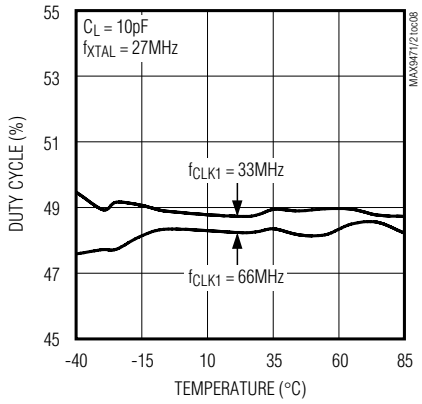
66MHz OUTPUT



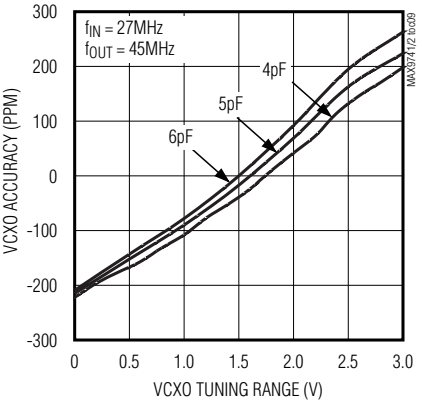
125MHz CLK OUTPUT



DUTY CYCLE vs. TEMPERATURE

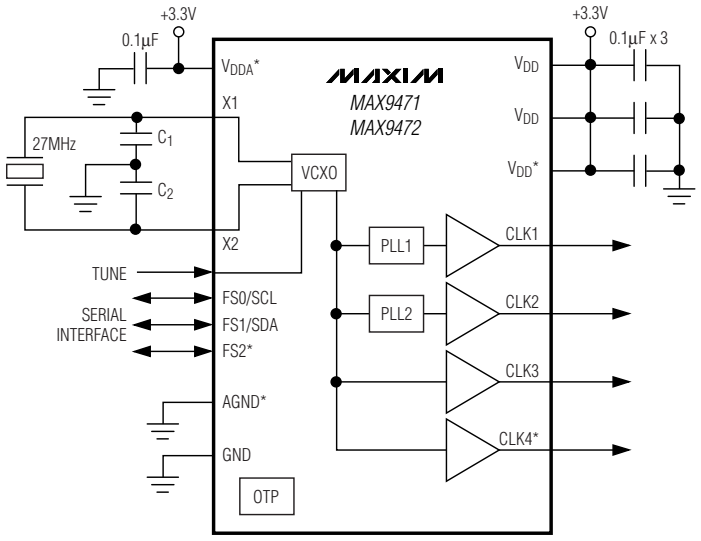


VCXO TUNING RANGE vs. VCXO ACCURACY



Multiple-Output Clock Generators with Dual PLLs and OTP

Typical Operating Circuit/Block Diagram



*MAX9471 ONLY.

Pin Description

PIN		NAME	FUNCTION
MAX9471	MAX9472		
1	5	TUNE	VCXO Tune Voltage Input. If using a reference clock input, connect TUNE to V_{DD}.
2	—	V_{DDA}	Analog Power Supply. Bypass to GND with a 0.1µF capacitor.
3	—	AGND	Analog Ground
4, 10, 11	6, 10, 11	GND	Ground
5	7	CLK1	Output Clock 1. PLL1 buffered output.
6	8	CLK2	Output Clock 2. PLL2 buffered output.
7	9	CLK3	Output Clock 3. VCXO buffered output.
8	—	CLK4	Output Clock 4. VCXO buffered output.
9	—	I.C.	Internally Connected. Leave unconnected.
12, 13, 16	4, 12	V_{DD}	Power Supply. Bypass to GND with a 0.1µF capacitor.
14	—	FS2	Function Select 2
15	13	$\overline{PD}$	Active-Low, Power-Down Input. Pull high for normal operation, drive $\overline{PD}$ low to place MAX9471/MAX9472 in power-down mode.
17	14	X2	Crystal Connection 2. Leave open if using a reference clock.
18	1	X1	Crystal Connection 1 or Reference Clock Input
19	—	FS0/SCL	Function Select 0/Serial Clock. Set FS2 high to place the device in I^2C mode (see Table 1).
20	—	FS1/SDA	Function Select 1/Serial Data. Set FS2 high to place the device in I^2C mode (see Table 1).
—	2	FS1	Function Select 1
—	3	FS0	Function Select 0
EP	—	EP	Exposed Pad (MAX9471 only). Connect EP to GND.

Detailed Description

The MAX9471/MAX9472 have two programmable fractional-N feedback PLLs so that almost any frequencies between 4MHz to 200MHz can be generated. The MAX9471 provides four outputs: two for the PLLs and two for the reference clock. The MAX9472 provides three outputs: two for the PLLs and one for the reference clock. The crystal frequency can be between 5MHz and 30MHz. The internal VCXO has a fine-tuning range of ±200ppm.

Power-Down

Driving $\overline{PD}$ low places the MAX9471/MAX9472 in power-down mode. $\overline{PD}$ overrides all other functions, setting all outputs to high impedance and shutting down the two PLLs. Every output has an 80kΩ (typ) internal pulldown resistor.

Voltage-Controlled Crystal Oscillator (VCXO)

The MAX9471/MAX9472s' internal VCXO produces a reference clock for the PLLs used to generate the output clocks. The oscillator uses a crystal clock as the base frequency reference and has a voltage-controlled tuning input for micro adjustment in a range of ±200ppm. The tuning voltage V_{TUNE} can vary from 0V to 3V as shown in Figure 1. The crystal should be AT cut and oscillate on its fundamental mode with ±30ppm accuracy. The crystal shunt capacitor should be less than 10pF, including board parasitic capacitance. To achieve up to ±200ppm pullability, the crystal-loading capacitance should be less than 14pF. The VCXO is a free-running oscillator. It starts oscillating with an internal POR signal and can be disabled by $\overline{PD}$. VCXO settles at approximately 5ms at power-on and 10µs at a change of the V_{TUNE} voltage.

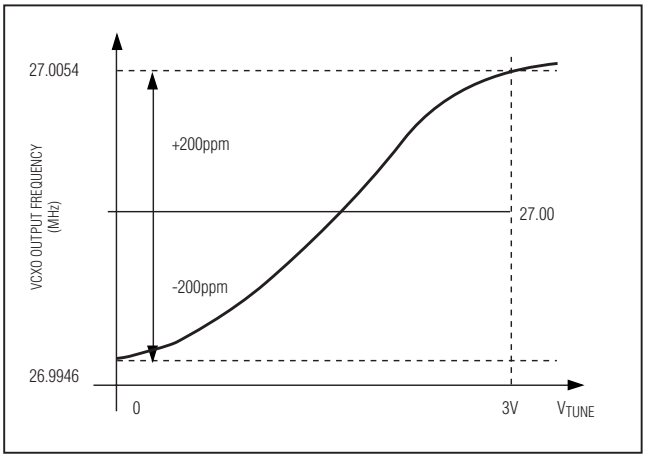


Figure 1. VCXO Tuning Range for a 27MHz Crystal

Choosing different C_1 and C_2 capacitors allows flexibility for centering the various crystals. See the *Typical Operating Characteristics* for an example.

To use the MAX9471/MAX9472 as a synthesizer with an input reference clock, connect the input clock to X1 and TUNE to V_{DD}, and leave X2 unconnected. This configuration is for applications where the micro tuning is not needed, and there is a system reference clock available.

One-Time Programmable Memory

The MAX9471/MAX9472 feature a factory-configurable, OTP memory for nonvolatile applications allowing for simple and permanent clock generation. Contact the factory for presetting the MAX9471/MAX9472 to requested frequencies.

Using OTP, the MAX9471/MAX9472 can be configured to two different configurations. One configuration is to have PLL1 set to any frequency between 4MHz to 200MHz and select the PLL2's frequency by I²C (MAX9471) or programmable pins. The second configuration is to preset the frequencies in PLL1 and PLL2 to fixed values between 4MHz to 200MHz. In both cases, the reference output is available, but it can be disabled by OTP. At power-up, all the outputs are enabled.

Frequency Selection of CLK2 Output

The OTP ROM can set PLL2's output to be selectable from a group of frequencies that are common for MPEG video and audio applications. The frequency selection can be done by the FS_ inputs or through the I²C interface (MAX9471). For the MAX9471, pull FS2 high (Table 1) to select the PLL2 frequency through the I²C interface. Otherwise, the frequencies are selected according to Table 2. For the MAX9471, Table 3 shows the mappings for I²C programming.

Serial Interface (MAX9471)

The MAX9471 can be programmed through a 2-wire, I²C-compatible serial interface. The device is activated after power-up and FS2 = high. The device operates as a slave that sends and receives data through clock line SCL and data line SDA for bidirectional communication with the master. A master (typically a microcontroller) initiates all data transfers to and from the MAX9471 and

Table 1. Mode Selection by FS2 (MAX9471 Only)

FS2	MODE
Low or open	Pin programmable
High	I²C enabled

Multiple-Output Clock Generators with Dual PLLs and OTP

Table 2. MAX9471/MAX9472 Frequency Selection at CLK2

FS2	FS1	FS0	FREQUENCY (MHz)
AUDIO FREQUENCIES			
Open	Open	Open	4.096
Open	Open	Low	6.144
Open	Open	High	8.1920
Open	Low	High	11.2896
Open	Low	Open	12.2880
Open	Low	Low	16.3840
Open	High	High	22.5792
Open	High	Open	24.5760
Open	High	Low	9.216
Low	Open	High	16.9344
Low	Open	Open	18.4320
Low	Open	Low	33.8688
Low	High	High	36.864
VIDEO FREQUENCIES			
Low	Low	Low	74.1758241
Low	Low	High	74.25
Low	Low	Open	54.054
High	X	X	Disable three-level pins and enable I²C

**MAX9472 can be programmed to FS2 = open settings only.*

Table 3. MAX9471 I²C Frequency Selection at CLK2 (FS2 = High)

A4	A3	A2	A1	FREQUENCY (MHz)
AUDIO FREQUENCIES				
0	0	0	0	4.096
0	0	0	1	6.144
0	0	1	0	8.1920
0	0	1	1	11.2896
0	1	0	0	12.2880
0	1	0	1	16.3840
0	1	1	0	22.5792
0	1	1	1	24.5760
1	0	0	0	9.216
1	0	0	1	16.9344
1	0	1	0	18.4320
1	0	1	1	33.8688
1	1	0	0	36.864
VIDEO FREQUENCIES				
1	1	0	1	74.1758241
1	1	1	0	74.25
1	1	1	1	54.054

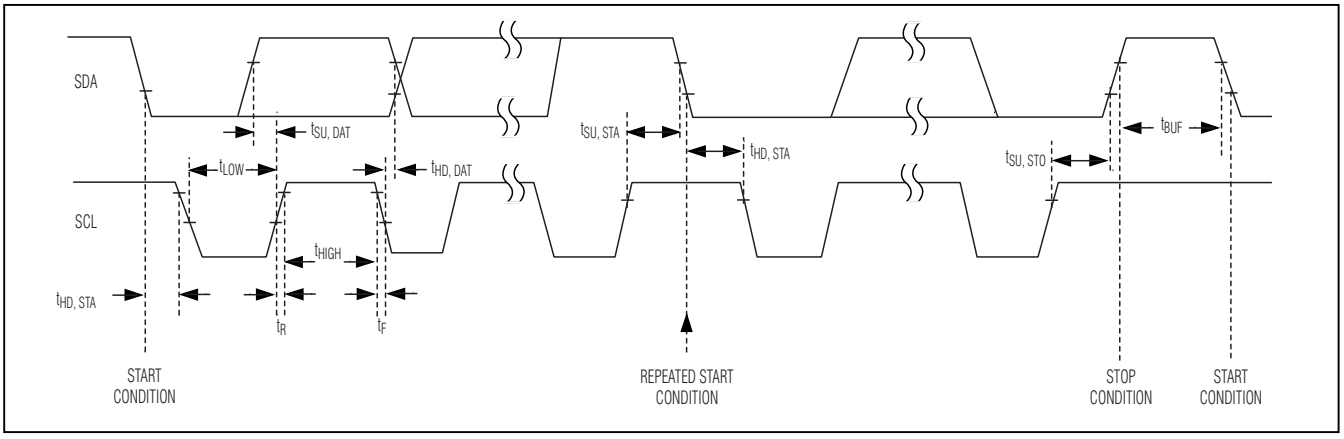


Figure 2. I²C Timing Diagram

generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. The SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire bus, or if the master in a single-master system has an open-drain SCL output. Figure 2 is the I²C timing diagram.

Device Address

The default I²C address for the MAX9471 is factory set to 1100111. Contact factory for different addresses.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. The active master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 3).

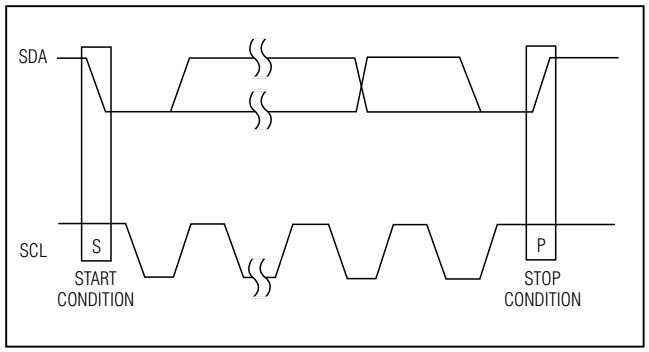


Figure 3. START and STOP Diagram

Data Transfer and ACK

Following the START condition, each SCL clock pulse transfers 1 bit. Between a START and a STOP, multiple bits are transferred on the 2-wire bus. The first 7 bits are for the device address. Bit 8 indicates the writing (low) or reading (high) operation (R/$\overline{W}$). Bit 9 is the ACK for the address and operation type. The next 8 bits (bit 10 to bit 17) form the content byte. The next bit, bit 18, is the ACK for the content byte. The master always transfers the first 8 bits (address + R/$\overline{W}$). The slave (MAX9471) may receive a content byte from the bus or transfer a content byte to the bus. The ACK bits are transmitted by the address or content recipient. A low-ACK bit indicates a successful transfer; otherwise, a high-ACK bit indicates an unsuccessful transfer. More content bytes can be continuously transferred until the master sends a STOP. For the MAX9471 data writing, after the 9 bits with the slave ID, R/$\overline{W}$, and ACK, 1 data byte is sent to the MAX9471 from the master. Figure 4 shows the structure of the data transfer. Figure 5 shows CLK_ rise and fall times.

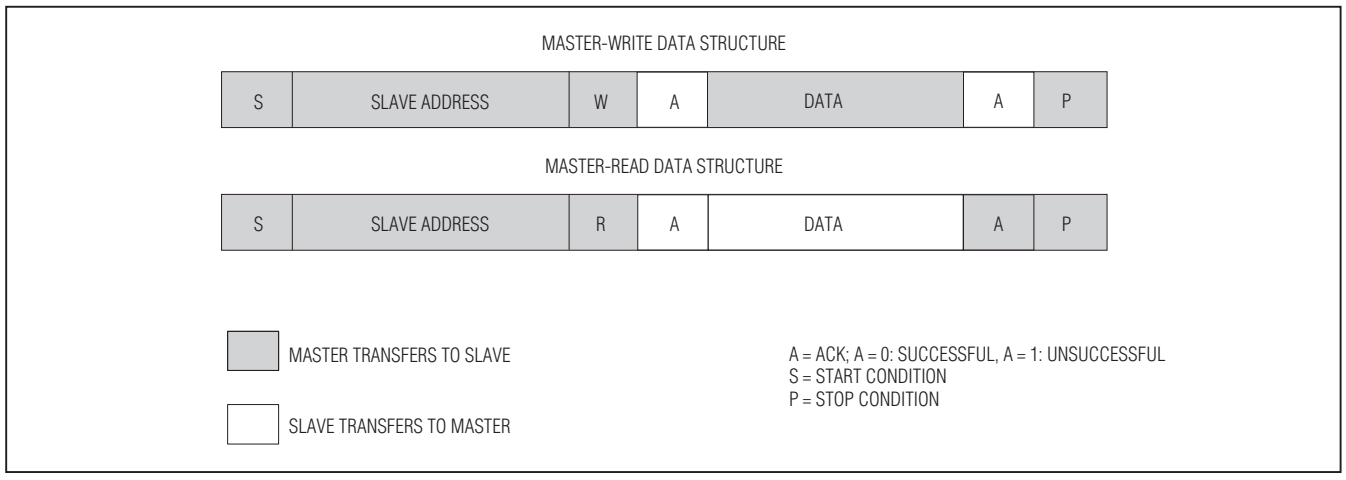


Figure 4. Serial-Interface Data Structure

Multiple-Output Clock Generators with Dual PLLs and OTP

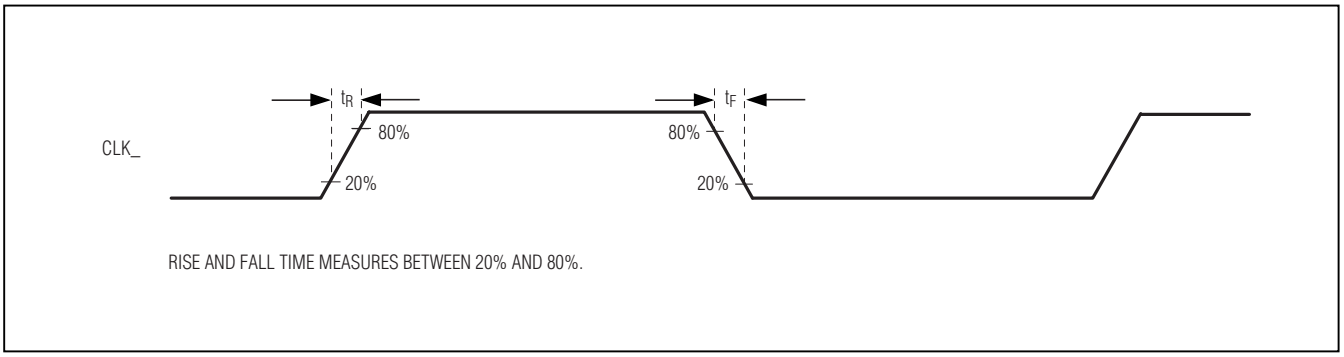


Figure 5. CLK_ Rise and Fall Times

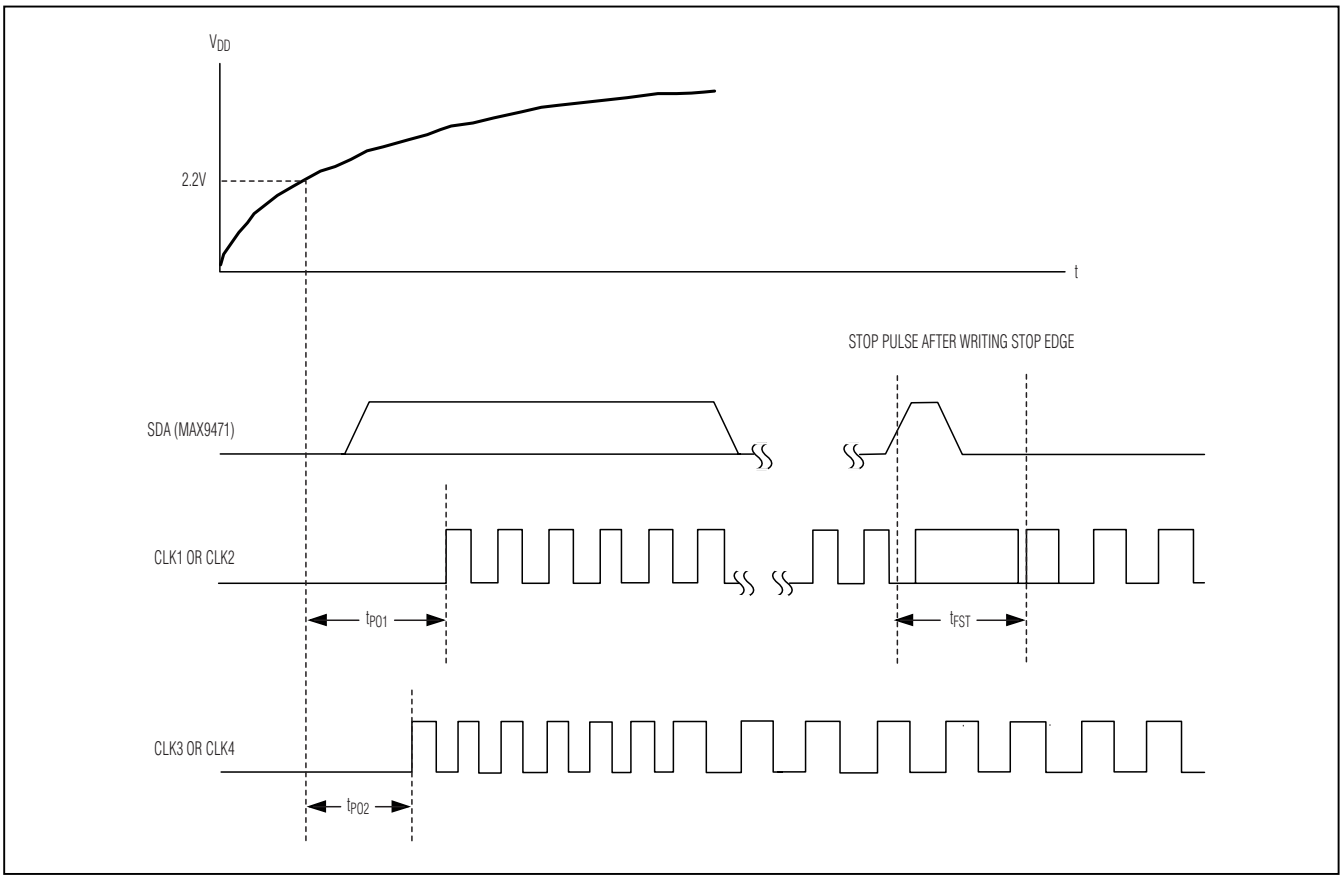


Figure 6. VCXO and PLL Timing Diagram

Applications Information

Crystal Selection

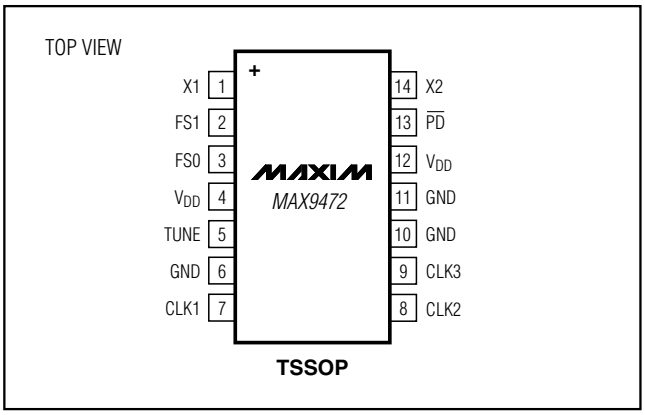
When using a crystal with the MAX9471/MAX9472s' internal oscillator, connect the crystal to X1 and X2. Choose an AT-cut crystal that oscillates on its fundamental mode with ±30ppm and loading capacitance less than 14pF. To achieve a wide VCXO tuning range, select a crystal with motional capacitance greater than 7fF and connect 6pF or less shunt capacitors at X1 and X2 to ground. When the VCXO is used as an oscillator, select both shunt capacitors to be approximately 13pF. The optimal shunt capacitors for achieving minimum frequency offset can be determined experimentally.

Board Layout Considerations and Bypassing

The MAX9471/MAX9472s' oscillator frequencies make proper layout important to ensure stability. For best performance, place components as close as possible to the device.

Digital or AC transient signals on GND can create noise at the clock output. Return GND to the highest quality ground available. Bypass each V_{DD} and V_{DDA} with a 0.1µF capacitor, placed as close as possible to the device. Careful PC board ground layout minimizes crosstalk between the outputs and digital inputs.

Pin Configurations (continued)



Chip Information

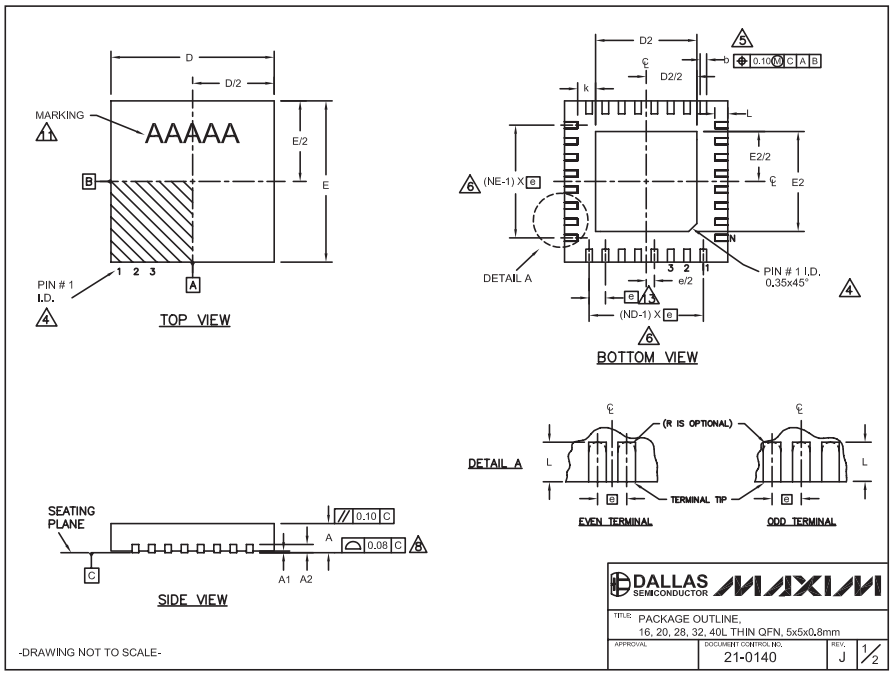
PROCESS: CMOS

Multiple-Output Clock Generators with Dual PLLs and OTP

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			----		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

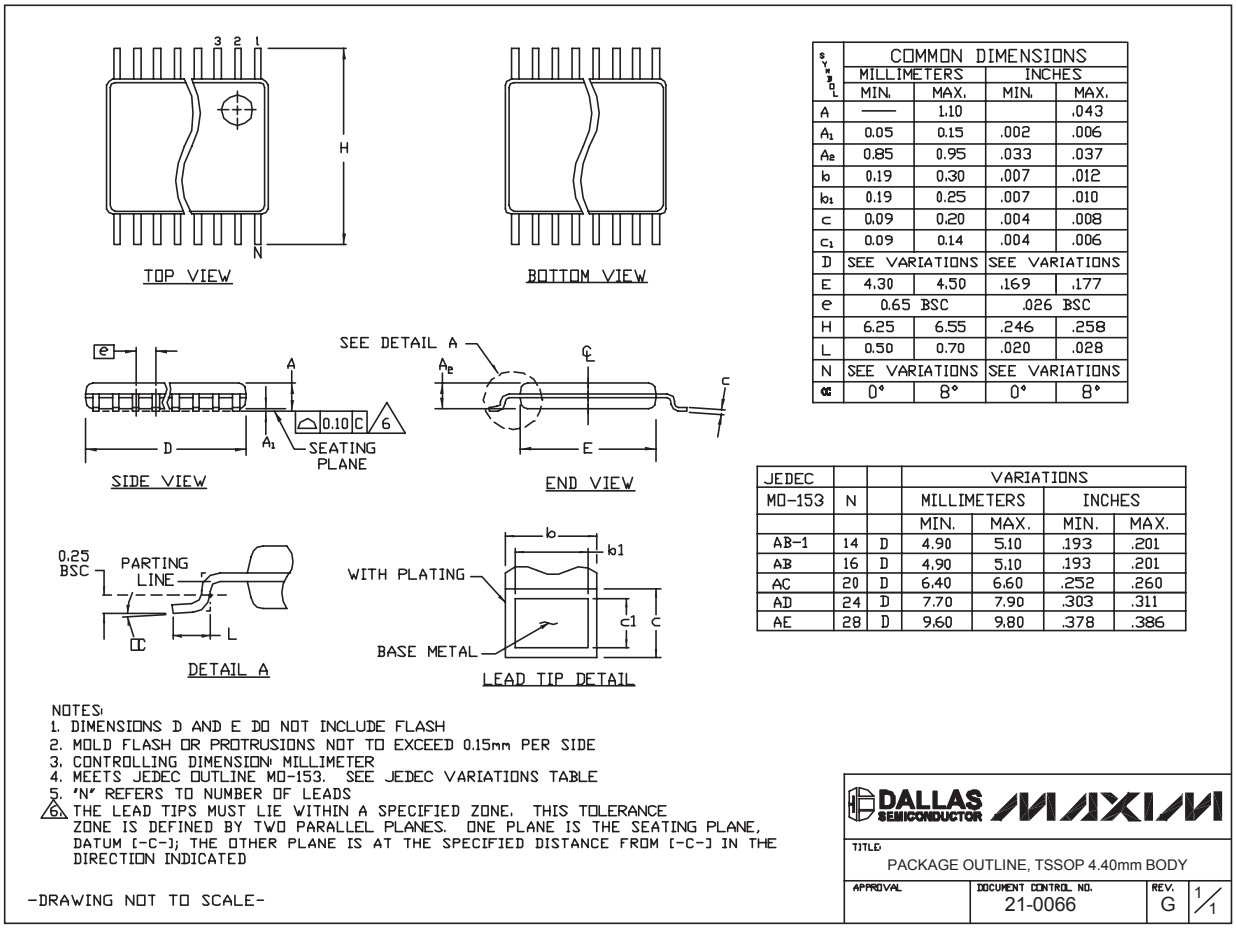
-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm
21-0140
J
2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	G	1/1

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

© 2006 Maxim Integrated Products MAXIM is a registered trademark of Maxim Integrated Products, Inc.